RADIATION TOLERANT INTELLIGENT MEMORY STACK

RTIMS FLASH MODULE
RADIATION HARDENED DESIGN

3DSS24G08VS3626

KEY FEATURES

- Single 3.3V Power Supply
- Up to 24 Gb of Space qualified NAND Flash Memory
  - 8 Gb with TMR memory protection
  - 16 Gb with EDAC memory protection
  - 24 Gb with no additional memory protection
- SLC memory technology
- Bad Block Free - continuous logic sectors
- 100 Kcycles Program/Erase endurance
- 10 years data retention
- Standard 8-bit NAND Flash I/F
- Access Time:
  - Write mode at 99 Mbits/s, Read mode at 287 Mbits/s
- Operating Temperature Range: -40°C/+105°C
- Radiation Hardened design:
  - Total Irradiation Dose(TID): > 50Krad(Si)
  - Single Event Latch-up(SEL) Immune > 80Mev.cm^2/mg
  - Single Event Upset(SEU) Immune by design
  - High Current Single Event Functional Interrupt (HC SEFI) Immune by design
- ITAR Free Product - Worldwide delivery guaranty
- Space Qualified Technology
- 38-pin SOP pitch 1.27mm
- Dimensions (Lxlxh): 31 x 28 x 11.2 mm & Mass: 16 gr.

PRODUCT OVERVIEW

The NAND Flash Radiation Tolerant and Intelligent Memory Stack (RTIMS FLASH) is a user-friendly, plug-and-play, radiation protected high density NAND Flash Memory. It provides a very high density, radiation hardened by design (RHBD), non-volatile memory module suitable for many space applications such as geo-stationary missions, earth observation, navigation, manned space vehicles and deep space scientific exploration.

The RTIMS embeds three non-volatile NAND Flash memories and one intelligent Flash Memory Controller (FMC). All of the basic devices embedded in the RTIMS are SEL Immune. Protection against high current SEFIs is performed by current detection and power switch electronics controlled by the FMC. The FMC also provides the module with full protection against SEU: Error Detection and Correction (EDAC) or Triple Modular Redundancy (TMR). The SEU protection can be selected between EDAC and TMR or switched off, and the effective RTIMS Flash density will be 8Gb in TMR protection, 16Gb in EDAC protection and 24Gb in the SEU protection off configuration.

The 3DSS24G08VS3626 offers continuous logic sectors (no bad blocks) and high added value functionalities such as wear leveling and memory self-test, as well as internal registers for telemetry information:

- Error free guaranteed sector 0 for Boot data storage
- Continuous logic sectors - Embedded Bad blocks management
- Embedded dynamic wear leveling function
- Embedded format, fetch failing block, sector logic generation commands for initialization
- Internal registers for configuration, operation status and telemetry information

And all these functionalities are fully configurable via H/W configuration pins and a powerful User Interface Port.

Thanks to its standard NAND FLASH interface, the 3DSS24G08VS3626 can easily be connected to any existing microprocessor or FPGA with an embedded NAND Flash interface. Its embedded high level functions also allow using it as a standalone small local data recorder.

PIN DESCRIPTION

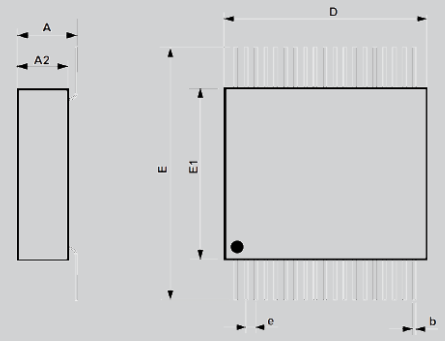
PIN	INPUT/OUTPUT	DESCRIPTION
		USER FLASH PIN
Vcc	I	Power Supply for device
GND	I	Ground Pin
R_B	O/Z	READY/BUSY indicates the status of the device operation
CE#	I	Chip Enable, active low
CLE	I	Command Latch Enable
ALE	I	Address Latch Enable
WE#	I	Write Enable, active low
RE#	I	Read Enable, active low
IO(7:0)	I/O	Input command, address and data, and to output data during read operations
WP#	I	Write Protect, active low
		CONFIGURATION PIN
ITACK_SPICLK	I	Acknowledge Interrupt / SPI clock
BBACK_SPICS#	I	Accept the new bad block / SPI Chip Select
IT0_SPIMOSI	I/O	Memory full interrupt / Data from Master to Slave
IT1_SPIMISO	O/Z	Bad block detected interrupt/Data from Slave to Master(To allow several SPI slaves connected to the same master)
IT2	O	Internal Counter overflowed interrupt/Global interrupt, active high
MEM_AR(1:0)	I	Triple Redundancy Mode / EDAC Mode / Full memory Mode
WL_EN	I	Dynamic Wear Leveling Enable
AD(4:0)	I	Component Address, used for SPI
SPI_EN	I	Wired configuration interface / SPI interface
RST#	I	Hardware reset, active low

ENVIRONMENT SPECIFICATIONS

PARAMETER	CONDITIONS	MIN	MAX	UNIT
TID	-	50		Krad(Si)
SEL	-	80		Mev.cm^2/mg
HC SEFI	-	Immune by design		Mev.cm^2/mg
SEU (TMR Mode)	LEO (1336km, 66°)		9.4E-26	error/bit/year
SEU (EDAC Mode)	LEO (1336km, 66°)		1.7E-25	error/bit/year

PARAMETER	CONDITIONS	REMARKS
Thermal Cycles	Mil-std-883 Method 1010 Condition B	500 Cycles, -55°C/+125°C
High Temperature Storage	Mil-std-883 Method 1008 JESD22-A103-A	2000hrs, 150°C
Shock	Mil-std-883 Method 2002 Condition B	Y1, 0.5 ms, 1500g
Sinusoidal Vibration	Mil-std-883 Method 2007 Condition A	peak acceleration 20g – 3 axes
Random Vibration	Mil-std-883 Method 2026 Condition I	Level H/J
HAST	JEDEC STD 22TMA110	264 hrs, +110°C
Outgazing	ESA-PSS-01-702 MA	TML&RML<1%, CVCM<0,1%

PACKAGE



	Min	Max
A	10.90	11.60
A2	9.80	10.20
D	27.80	28.20
E	30.70	31.10
E1	27.90	28.10
b	0.35	
e	1.27	
Dimension (mm)		

Max. weight : 16 gr.

TEMPERATURE RANGES

C : Commercial (0°C to 70°C)

I : Industrial (-40°C to +85°C)

S : Specific (-40°C to +105°C)

QUALITY GRADES

N : Commercial

B : Industrial

S : Space

ORDERING INFORMATION

Quality Grade — Options

Part Number – X X – X00X

Temperature Range

3D PLUS a HEICO company

www.3d-plus.com