Radiation Intelligent Memory Controller

DDR4 SDRAM Controller IP Core

3DIPMC0815-1

GENERAL DESCRIPTION

The Radiation Intelligent Memory Controller (RIMC DDR4) is a fully configurable DDR4 SDRAM memory controller IP core designed to operate with 3D PLUS DDR4 memory modules to achieve radiation tolerance improvement. The RIMC contains all standard functions of a DDR memory controller for bus width applications from 8b up to 80b according to PHY limitation. It also includes additional functions, such as Single Event Upset (SEU) mitigation and Single Event Functional Interrupt (SEFI) correction to operate in radiation environments.

In addition to the memory controller IP within the RIMC IP core, the user can either select PHY IPs provided in the IP core or develop his own PHY IP.

The RIMC has two primary interfaces, the user interface (UIF) and the DDR memory interface (DFI).

The UIF features an AHB bus, an AXI bus or UPI, and an APB bus for user dynamic configuration:

Slave APB interface dedicated to internal registers,
Optional slave AHB/AXI interface,
Optional Bypass interface,
Optional UPI interface (interface compatible with MIG from Xilinx).

Thanks to this interface subsystem, the user is able to use DDR4 SDRAM memories in his design without having to focus on the complex mechanisms required to work in a harsh environment.

KEY FEATURES

- Compatible with all 3D PLUS SDRAM DDR4 module
- SEFI protection and SEU mitigation
- Configurable memory bus width from 8 to 80 bits
- Configurable via AMBA user interface, compliant AXI/AHB/APB
- DDR4 PHY interface compliant DFI 3.1
- Rank and bank management algorithms
- Dynamically configurable via an 8-bit APB slave interface
- Direct access to memories provided by the controller Bypass mode
- Selectable Hamming or Reed-Solomon Error Correction Code (ECC)
- Configurable DDR4 ranks to increase memory density
- Clock & ODT settings compatible with 3D PLUS modules
- Burst-of-8 accesses for DDR4 interface
- Selectable Enable/Disable of DDR4 scrubbing
- User-definable scrubbing frequency
- Selectable or autocalibration of SDRAM DDR4 refresh time

FPGA TARGET RIMC

The RIMC SDRAM DDR4 is targeting the following FPGA devices :

- XILINX Kintex Ultrascale
- MICROCHIP PolarFire
- XILINX Kintex UltraScale+

RIMC INTERFACE SUBSYSTEM